

ABSTRACT OF THE DISCLOSURE

Disclosed herein are a semiconductor method and device which are capable of reducing data write errors by rewriting last write data during a write recovery time (tWR).

5 The semiconductor device comprises a memory cell array consisting of a plurality of repetitive cell units; a bit line amplifier for amplifying a voltage difference between a bit line voltage and a complementary bit line voltage of the memory cell array; switching devices activated by a column selection line signal for electrically connecting a data line and a complementary data line to the bit line and the complementary bit line, respectively; and a write driver for
10 supplying a write data voltage to the data line and the complementary data line, wherein the column selection line signal is generated during a write recovery time. The method for controlling the semiconductor device including a memory cell array having a plurality of repetitive cell units, a bit line amplifier for amplifying a voltage difference between a bit line voltage and a complementary bit line voltage of the memory cell array, switching devices
15 activated by a column selection line signal for electrically connecting a data line and a complementary data line to the bit line and the complementary bit line, respectively, and a write driver for supplying a write data voltage to the data line and the complementary data line, comprises the steps of: writing data voltage into the memory cell array; and generating the column selection line signal during a write recovery time.

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